ABSTRACT OF THE DISCLOSURE

A reconfigurable system for performing a set of arithmetic operations. The reconfigurable system may have a frame buffer, an accumulation buffer and a pixel computation unit. The pixel computation unit includes a control unit and one or more copies of a reconfigurable circuit. The reconfigurable circuit may include a subtractor, a multiplier, an adder, and a set of multiplexors. The control logic drives selects lines of the set of multiplexors in the one or more circuit copies through one or more computational cycles in order to implement a programmable operation (such as scale and/or bias, accumulate, dynamic blend and matrix multiply). The pixel computation unit may receive pixels values from one or more sources including the frame buffer and the texture buffer, and operate on the pixels using the one or more circuit copies to generate a stream of output pixels.